

WHAT IS CLAIMED IS:

1           1.       A method of forming a simultaneous operation dual-bank flash  
2 memory device, said method comprising the steps of:  
3           providing a plurality of flash memory arrays;  
4           providing row and column decoders for each flash memory array; and  
5           partitioning the plurality of flash memory arrays into a first memory bank and  
6 a second memory bank by coupling first bank row and column address lines between first  
7 bank row and column pre-decoders and the row and column decoders associated with the first  
8 memory bank, and by coupling second bank row and column address lines between second  
9 bank row and column pre-decoders and the row and column decoders associated with the  
10 second memory bank.

1           2.       A method of forming a dual-bank flash memory device, said method  
2 comprising the steps of:  
3           providing a plurality of flash memory arrays, each memory array having  
4 associated row and column address decoders; and  
5           partitioning the flash memory arrays into a first memory bank and a second  
6 memory bank by:  
7               forming first bank pre-decoded column address lines and coupling  
8 them between a first bank column address pre-decoder and the column address  
9 decoders associated with the first bank,  
10           forming second bank pre-decoded column address lines and coupling  
11 them between a second bank column address pre-decoder and the column address  
12 decoders associated with the second bank,  
13           forming first bank pre-decoded row address lines and coupling them  
14 between a first bank row address pre-decoder and the row address decoders associated  
15 with the first bank, and  
16           forming second bank pre-decoded row address lines and coupling them  
17 between a second bank row address pre-decoder and the row address decoders  
18 associated with the second bank.

1           3.       The method of claim 2, wherein the sizes of the first and second  
2 memory banks are variable, depending upon selection from and application of one a plurality  
3 of preformed metal masks used to perform the step of partitioning.

4                   4.       The method of claim 3, wherein each memory array comprises first  
5   and second halves, the first half having an associated column decoder and the second half  
6   having an associated column decoder.

1                   5.       A simultaneous operation flash memory chip having a flexible memory  
2   bank partition, comprising:

3                   a plurality of memory arrays having associated row and column decoders, said  
4   plurality of memory arrays partitioned into first and second memory banks;

5                   a first bank column address pre-decoder coupled to the column address  
6   decoders associated with the first memory bank;

7                   a first bank row address pre-decoder coupled to the row address decoders  
8   associated with the first memory bank;

9                   a second bank column address pre-decoder coupled to the column address  
10   decoders associated with the second memory bank; and

11                   a second bank row address pre-decoder coupled to the row address decoders  
12   associated with the second memory bank.

1                   6.       The simultaneous operation flash memory chip of claim 5, wherein the  
2   partition between the first and second memory banks is determined by selecting from a  
3   plurality of preformed metal masks and applying the selected mask during manufacture of the  
4   flash memory chip.

1                   7.       The simultaneous operation flash memory chip of claim 6, wherein the  
2   plurality of metal masks are distinguished from one other by variances in pre-decoded  
3   address line patterns.

1                   8.       The simultaneous operation flash memory chip of claim 7, wherein the  
2   pattern variances determine to which memory arrays pre-decoded first bank address lines are  
3   coupled to and to which memory arrays pre-decoded second bank address lines are coupled  
4   to.

1                   9.       A simultaneous operation flash memory device having a flexible dual-  
2   bank architecture, comprising: a plurality of memory arrays capable of being partitioned into  
3   a first memory bank and a second memory bank, the partitioning of arrays within the first and  
4   second memory banks determined by how pre-decoded row and address lines are formed  
5   during a process used to fabricate the device.

1                   10.     A method of forming a simultaneous operation flash memory device  
2     having a flexible memory bank partition, said method comprising the steps of:  
3                   providing a plurality of flash memory arrays, each memory array having  
4     associated row and column address decoders; and  
5                   partitioning the plurality of flash memory arrays into a first memory bank and  
6     a second memory bank by:  
7                   coupling first bank row and column address lines between first bank  
8     row and column pre-decoders and the row and column decoders associated with the  
9     first memory bank and  
10                  coupling second bank row and column address lines between second  
11     bank row and column pre-decoders and the row and column decoders associated with  
12     the second memory bank,  
13                  wherein the step of partitioning is performed by selecting from a plurality of  
14     preformed metal masks, said plurality of metal masks being distinguished from one other by  
15     variances in pre-decoded address line patterns.